What is claimed is:

[Claim 1] 1. A damascene method capable of avoiding copper extrusion, the damascene method comprising:

providing a semiconductor wafer including a substrate with at least one metal layer on the substrate;

depositing a dielectric layer on the metal layer;

forming a damascene recess structure having an opening exposing a portion of the metal layer in the dielectric layer;

performing a degas step to make gas escape from the dielectric layer;

forming a barrier layer on portions of the exposed surface of the metal layer and on the damascene recess structure; and

forming a conductive layer on the barrier layer.

[Claim 2] 2. The method of claim 1 wherein the gas escaping from the dielectric layer fluorine-containing gas.

[Claim 3] 3. The method of claim 1 wherein the degas step is an anneal step by heating to a range between 200℃ to 300℃.

[Claim 4]

4. The method of claim 1 wherein a passivation layer is formed between the metal layer and the dielectric layer.

[Claim 5] 5. The method of claim 4 wherein the passivation layer is substantially made from silicon nitride.

[Claim 6] 6. The method of claim 1 wherein the dielectric layer is a laminate compound layer comprising a first low-k dielectric, a stop layer over the first low-k dielectric, a second low-k dielectric, and a hard mask layer.

[Claim 7] 7. The method of claim 1 wherein the metal layer is made of copper or tungsten.

[Claim 8] 8. The method of claim 1 wherein the damascene recess structure is a dual damascene recess.

[Claim 9] 9. A damascene method capable of avoiding conductive material extrusion, the damascene method comprising:

providing a substrate;

forming a plurality of devices on the substrate;

forming an interlayer dielectric to encapsulate the plurality of devices;

forming a plurality of conductive plugs in the interlayer dielectric to connect the devices on the substrate;

forming a dielectric layer having an embedded metal layer therein over the interlayer dielectric;

forming a low-k dielectric film over the dielectric layer;

etching a damascene recess structure in the low-k dielectric film, the damascene recess structure communicating the embedded metal layer;

executing a degas step to expel gas contained by the low-k dielectric film;

forming a barrier layer covering surface of the damascene recess structure and surface of the low-k dielectric film; and

depositing a conductive layer over the barrier layer.

[Claim 10] 10. The method of claim 9 wherein the gas contained by the low-k dielectric film is fluorine-containing gas.

[Claim 11] 11. The method of claim 9 wherein the degas step is an annealing step executed within a temperature range between 200℃ to 300℃.

[Claim 12]

12. The method of claim 9 wherein the conductive layer is a copper layer.

[Claim 13] 13. The method of claim 9 wherein between the embedded metal layer and the low-k dielectric layer, a passivation layer is formed.

[Claim 14] 14. The method of claim 13 wherein the passivation layer is substantially made from silicon nitride.

[Claim 15] 15. The method of claim 9 wherein the low-k dielectric layer has a dielectric constant (k) that is less than 2.9.

[Claim 16] 16. The method of claim 9 wherein the low-k dielectric film is a laminate compound layer comprising a first low-k dielectric, a stop layer over the first low-k dielectric, a second low-k dielectric, and a hard mask layer.

[Claim 17] 17. The method of claim 9 wherein the damascene recess structure is a dual damascene recess.